CLAIMS

I Claim:

1. A method of transferring data using a field programmable gate array (FPGA), the method comprising:

retrieving a first set of data from a first section of a configuration memory of the FPGA;

storing the first set of data retrieved from the first section of the configuration memory in a first storage element;

transferring the first set of data from the first storage element directly to a second storage element on a configuration bus of the FPGA; and

transferring the first set of data from the second storage element to a second section of the configuration memory of the FPGA.

2. The method of Claim 1, further comprising loading the first set of data into the first section of the configuration memory on the configuration bus.

3. The method of Claim 1, wherein the first set of data comprises data stored in a single column of the configuration memory.

4. The method of Claim 1, wherein the step of retrieving the first set of data comprises retrieving the first set of data from the first section of the configuration memory in parallel.

5. The method of Claim 4, wherein the step of transferring the first set of data from the first storage element to the second storage element comprises shifting the first set of data onto the configuration bus as a plurality of data words.

6. The method of Claim 5, wherein each of the data words and the configuration bus have a width of 32-bits or greater.

7. The method of Claim 1, further comprising write-protecting one or more selected regions of the second section *of the configuration memory*.

8. The method of Claim 1, further comprising:

loading an address associated with the first section of the configuration memory into a first address register; and

loading a second address associated with the second section of the configuration memory into a second address register.

9. The method of Claim 8, further comprising:

loading an instruction specifying a data transfer into a command register.

10. The method of Claim 9, further comprising providing an instruction specifying the number of words in the first set of data.

11. A field programmable gate array (FPGA) comprising:

a configuration memory arranged in rows and columns;

a configuration bus configured to route data to and from the configuration memory, the configuration bus having a first width;

a source frame address register configured to store a source frame address that identifies a source section in the configuration memory;

a destination frame address register configured to store a destination frame address that identifies a destination section in the configuration memory;

a command register configured to receive a copy configuration instruction; and

configuration logic configured to transfer data from the source section to the destination section in response to the copy configuration instruction in the command register.

12. The FPGA of Claim 11, wherein the configuration logic comprises a data path for routing the data from the source section to the destination section, wherein the data path has a width at least as wide as the first width.

13. The FPGA of Claim 12, wherein the data path comprises the configuration bus.

14. The FPGA of Claim 12, wherein the data path further comprises:

a frame data output register configured to receive data from the source section address of the configuration memory; and

a frame data input register configured to receive the data from the frame data output register via the configuration bus, and provide the data to the destination section address of the configuration memory.

15. The FPGA of Claim 12, wherein the configuration logic further comprises a configuration state machine configured to control the data path in response to the source frame address, the destination frame address and the copy configuration instruction.

16. The FPGA of Claim 11, further comprising a plurality of write-protect configuration memory cells coupled to the configuration memory.

17. The FPGA of Claim 11, wherein the source section is a source column in the configuration memory, and wherein the destination section is a destination column in the configuration memory.

18. A field programmable gate array (FPGA) comprising:

means for retrieving a first set of data from a first section of a configuration memory of the FPGA;

means for storing the first set of data retrieved from the first section of the configuration memory;

a configuration bus configured for transferring the first set of data from the means for storing the first set of data directly to a second means for storing the first set of data; and

means for transferring the first set of data from the second means for storing the first set of data to a second section of the configuration memory of the FPGA.

19. The method of Claim 18, wherein the first set of data comprises data stored in a single column of the configuration memory.

20. The method of Claim 18, wherein the means for retrieving the first set of data comprises means for retrieving the first set of data from the first section of the configuration memory in parallel.

21. The method of Claim 20, wherein the means for transferring comprises means for shifting the first set of data onto the configuration bus as a plurality of data words.

22. The method of Claim 18, further comprising means for write-protecting one or more selected regions of the second section of the configuration memory.